

## US Patents Awarded:

1. Deep Bera, **B.S. Raghavendra**, Rangavittal Narayanan, Sandipan Chakroborty, Praveen Pankajakshan, **Method and apparatus for classifying cardiac arrhythmia**, US Patent, Patent No.: US 9,380,956 B2, Date of Patent: Jul. 5, 2016.
2. Shekhar Ramachandra Borgaonkar, Prasenjit Dey, **Deepu VIJAYASENAN**, "**Systems and methods for estimating distances using multi-resolution functions**", US 20090204364 A1, Publication date 5 Jun 2012. (Deepu Vijayasenana is currently with the dept. of E&C Engg., NITK Surathkal). *Patent ownership is with Hewlett- Packard Development Company, L.P., USA*
3. Dinesh Mandalapu, Anjaneyulu Seetha Rama Kuchibhotla, Sriganesh Madhvanath, **Deepu VIJAYASENAN**, Rama Vennelakanti, "**Annotation on media sheet indicating functionality to be performed in relation to image on media sheet**", US 8482827 B2, Publication date Jul 9, 2013. (Deepu Vijayasenana is currently with the dept. of E&C Engg., NITK Surathkal). *Patent ownership is with Hewlett-Packard Development Company, L.P., USA*

## US patents Filed:

1. **T Laxminidhi and Hareesh P. K.** , "A Process Insensitive CMOS Based Current reference" filed by Cadence Design Systems, Bangalore in December 2015.
2. Omprakash, **M.S. Bhat, Sumam David and U. Sripathi**, "*Alternative means for conductor based short distance signal/data transfer*", (Pub. No WO/2009/136414, Pub Date 12-11-2009, Intl. Appln No, PCT/IN2009/000257 Intl. Filing Date 29-04-2009).

## Indian Patents Granted:

1. Patent No. 301828 (Oct. 2018) - *Alternative means for conductor based short distance signal/data transfer*. Inventors: **Omprakash, M.S. Bhat & U. Sripathi**, Application No. 1076/CHE/2008 on 30-04-2008.

## Indian Patents Filed:

1. Laxminidhi T., **M. Shankaranarayana Bhat** and Jagadish D. N., "*Switched Capacitor Integrator based Successive Approximation Register Analog to Digital Converter Circuit and Conversion Method Thereof*", filed at Indian Patent Office, Chennai – No. 3549/CHE/2014 on 18/06/2014. Publication date: 14/01/2016. Request for Examination date: 14/01/2016.
2. **M Shankaranarayana Bhat and Jagadish D. N.**, "*Successive Approximation Register Analog to Digital Converter Circuit and Conversion Method Thereof*" filed at Indian Patent Office, Chennai – No. 4777/CHE/2013 on 18/11/2013. Publication date: 24/04/2015. Request for Examination date: 15/05/2015.
3. **M Shankaranarayana Bhat and Jagadish D. N.**, "**SAR ADC**" filed at Indian Patent Office, Chennai – No. 2372/CHE/2013 on 30/05/2013. Publication date: 06/02/2015. Request for Examination date: 05/04/2017.
4. **U. Sripathi Acharya**, K. Rajesh Shetty, K. Ramakrishna, **Prashantha Kumar H**, "*Design and Construction of BCH Codes for Enhancing Data Integrity in Multi Level Flash Memories*", filed on 24-12-2010 at the Patent Office Chennai.(Application number 3/CHE/2011 dated 03-01-2011).

5. **U. Sripati Acharya, K Rajesh Shetty and Prashantha Kumar H**, “*Design and construction of Algebraic codes for enhancing data integrity in Flash Memory Devices*” – Patent filed on 09-10-2009 (No.2493/CHE/2009).
6. **U. Sripati Acharya and Myagmarbayar Nergui**, “*Reducing the effect of Channel Noise while transmitting or storing a Watermarked Image*” – Patent filed on 25-03-2009 (No. 743/CHE/2009).
7. **Omprakash, Sumam David** – “*Programmable Switch Network for swapping the connection between sets of nodes*” - Patent filed on 3-6-2008 (No. 1359/CHE/2008).